Claims

1. A localized split floating gate device, comprising:

a substrate having a first source-drain junction and a second source-drain junction;

a first oxide region defined over the first source-drain junction and a second oxide region defined over the second source-drain junction;

a first floating gate defined with an overlap over the first source-drain junction and adjacent to the first oxide region, the overlap capable of establishing a degree of drain coupling when the first source-drain junction is wired as a drain; and

a second floating gate defined with an overlap over the second source-drain junction and adjacent to the second oxide region, the overlap capable of establishing a degree of drain coupling when the second source-drain junction is wired as a drain.

2. A localized split floating gate device as recited in claim 1, further comprising a spacer on either side of the first oxide region, the spacer assisting in defining an amount of the overlap.

3. A localized split floating gate device as recited in claim 2, wherein the spacer is a silicon nitride spacer.

4. A localized split floating gate device as recited in claim 2, wherein the spacer is an oxide spacer.

5. A localized split floating gate device as recited in claim 1, further comprising a spacer on either side of the second oxide region, the spacer assisting in defining an amount of the overlap.

6. A localized split floating gate device as recited in claim 5, wherein the spacer is a silicon nitride spacer.

7. A localized split floating gate device as recited in claim 5, wherein the spacer is an oxide spacer.

8. A localized split floating gate device as recited in claim 1, further comprising:

an oxide layer over the first and second floating gates;

a tunnel oxide layer defined over the substrate; and

a polysilicon gate defined between the first floating gate, the second floating gate, and over the tunnel oxide layer, wherein a channel is defined in the substrate under the tunnel oxide layer.

9. A localized split floating gate device as recited in claim 1, wherein when the first source-drain junction is a drain, the second floating gate stores a first bit, and the first floating gate experiences the degree of drain coupling to suppress a second bit effect.

10. A localized split floating gate device as recited in claim 1, wherein the overlap ranges between about 0.01 micron and about 0.1 micron.

11. A localized split floating gate device as recited in claim 1, wherein the overlap ranges between about 0.03 micron and about 0.08 micron.

12. A localized split floating gate device as recited in claim 1, wherein the overlap is about 0.06 micron.

13. A localized split floating gate device, comprising:

a drain junction defined in a substrate;

an oxide region defined over a center region of the drain junction; and

a floating gate defined adjacent to the oxide region, the floating gate defined with an overlap over the drain junction, the overlap capable of establishing a degree of drain coupling to suppress a reverse read second bit effect.

14. A localized split floating gate device as recited in claim 13, further comprising a spacer on either side of the oxide region, the spacer assisting in defining an amount of the overlap.

15. A localized split floating gate device as recited in claim 14, wherein the spacer is a silicon nitride spacer.

16. A localized split floating gate device as recited in claim 14, wherein the spacer is an oxide spacer.

17. A localized split floating gate device as recited in claim 13, further comprising:

an oxide layer over the floating gate;

a tunnel oxide layer defined over the substrate; and

a polysilicon gate defined over the tunnel oxide layer and the oxide layer.

18. A localized split floating gate device as recited in claim 13, wherein the floating gate experiences a degree of drain coupling to suppress a second bit effect.

19. A localized split floating gate device as recited in claim 13, wherein the overlap ranges between about 0.01 micron and about 0.1 micron.

20. A localized split floating gate device as recited in claim 13, wherein the overlap ranges between about 0.03 microns and about 0.08 micron.

21. A localized split floating gate device as recited in claim 13, wherein the overlap is about 0.06 micron.

22. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation, comprising:

providing a substrate having a first source-drain junction and a second source-drain junction;

forming a first oxide region over the first source-drain junction and a second oxide region over the second source-drain junction;

forming a first floating gate with an overlap over the first source-drain junction and adjacent to the first oxide region, the overlap capable of establishing a degree of drain coupling when the first source-drain junction is wired as a drain; and

forming a second floating gate with an overlap over the second source-drain junction and adjacent to the second oxide region, the overlap capable of establishing a degree of drain coupling when the second source-drain junction is wired as a drain.

23. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, further comprising:

forming a spacer on either side of the first oxide region, the spacer assisting in defining an amount of the overlap.

24. A localized split floating gate device as recited in claim 23, wherein the spacer is a silicon nitride spacer.

25. A localized split floating gate device as recited in claim 23, wherein the spacer is an oxide spacer.

26. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, further comprising:

forming a spacer on either side of the second oxide region, the spacer assisting in defining an amount of the overlap.

27. A localized split floating gate device as recited in claim 26, wherein the spacer is a silicon nitride spacer.

28. A localized split floating gate device as recited in claim 26, wherein the spacer is an oxide spacer.

29. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, further comprising:

forming an oxide layer over the first and second floating gates;

forming a tunnel oxide layer over the substrate; and

forming a polysilicon gate between the first floating gate, the second floating gate, and over the tunnel oxide layer, wherein a channel is defined in the substrate under the tunnel oxide layer.

30. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, wherein when the

first source-drain junction is a drain, the second floating gate stores a first bit, and the first floating gate experiences the degree coupling to suppress a second bit effect.

31. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, wherein the overlap ranges between about 0.01 micron and about 0.1micron.

32. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, wherein the overlap ranges between about 0.03micron and about 0.08micron.

33. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 22, wherein the overlap is about 0.06micron.

34. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation, comprising:

forming a drain junction defined in a substrate;

forming an oxide region defined over a center region of the drain junction; and

forming a floating gate defined adjacent to the oxide region, the floating gate defined with an overlap over the drain junction, the overlap capable of establishing a degree of drain coupling to suppress a reverse read second bit effect.

35. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 34, further comprising:

forming a spacer on either side of the oxide region, the spacer assisting in defining an amount of the overlap.

36. A localized split floating gate device as recited in claim 35, wherein the spacer is a silicon nitride spacer.

37. A localized split floating gate device as recited in claim 35, wherein the spacer is an oxide spacer.

38. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 34, further comprising:

forming an oxide layer over the floating gate;

forming a tunnel oxide layer over the substrate; and

forming a polysilicon gate over the tunnel oxide layer and the oxide layer.

39. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 34, wherein the floating gate experiences a degree of drain coupling to suppress a second bit effect.

40. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 34, wherein the overlap ranges between about 0.01micron and about 0.1micron.

41. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 34, wherein the overlap ranges between about 0.03micron and about 0.08micron.

42. A method for making a localized split floating gate device having second bit effect suppression in a reverse read operation as recited in claim 34, wherein the overlap is about 0.06micron.